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A Novel High-Frequency PLL Design for wireless applications

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Nowadays, there are growing trends of advances in wireless devices and becoming common in every household and workplace. The increasing desire for these devices is to create smaller, fast, and low power applications. The growing need in today s wireless applications is increasing requirements for identification of a high-speed low noise, low power novel Phase-locked loop (PLL) design. The PLL feedback loop can be found in nearly all aspects of wireless communication, these include radio, TV, cell phones, PDAs, pagers, wireless transmitters and receivers, etc. Phase-locked loop (PLL) is a feedback control system that generates an output signal whose frequency and phase depends on the phase of the input signal, the main PLL building blocks are; Phase Frequency Detector (PFD), Charge Pump (CP), Loop Filter (LF), Voltage Controlled Oscillator (VCO), and Frequency Divider (FD). This paper addresses a wide tuning range "2.4-5.0 GHz", novel high-frequency PLL design for wireless applications. The theoretical model and PLL analysis are principally described in the theoretical part. While, in the practical part, the design choices of various blocks, design calculation and simulation for final solutions are presented. The novel designed solution is simulated using 22nm CMOS technology, SPICE simulation software is used to evaluate the theoretical basics and fundamentals, and the final result are commented.

Keywords: Novel PLL Design; 22 nm Technology, Wireless Applications.

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1. Introduction

In recent years, wireless devices such as radio, TV, cell phones, PDAs, pagers, wireless transmitters and receiver's cell phones, etc are growing rapidly and becoming more popular, necessitating a variety set of features. This prosperity in popularity will only continue to increase with new CMOS technology structures and novel CMOS circuit designs [1].

The PLL circuit is existing widely in high-frequency applications and wireless devices, from simple clock circuits up to internal and oscillator circuits as a functional building electronic block. It has four major blocks: PFD, CP, LF, VCO, and FD. PLLs are obtained under two conditions; when the delay line is closed in a ring topology of the VCO, this is generally controlled by passed current through the loop, and the oscillator frequency is controlled by the PLL feedback loop. The loop generates accurate output as a frequency or time-dependent signals. The PLL loop has three different states, free running, capture, and phase lock; with no input signal, the PLL is said to be in free running state before the input is applied, on the occasion of the applied input signal, the oscillator generated frequency starts to adjust and PLL is labelled as the capture mode, when the comparison is in steady-state, phase and frequency of the output signal is matched to that of the incoming signal, it termed that, the PLL is in lock state. If the two signals differ in phase/frequency, an error voltage is generated in a repetitive action to reach lock state. The PLL frequency ranges are shown in Fig.1 [2].

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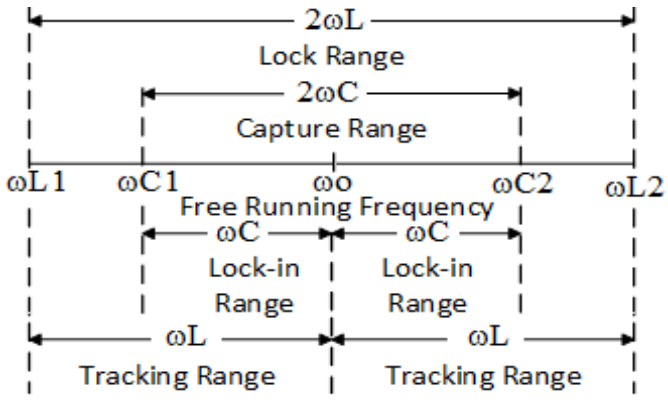

Fig.1. The PLL frequency ranges

Where; ωo is the centre frequency, ω_C is the lock-in range, ω_L is the tracking range, $2\omega_C$ is the capture range, and $2\omega_L$ is the lock range.

The main challenge of a novel PLL design is in the use of circuit level; fully integrated 22 nm CMOS technology, and this is clearly demonstrated in the simulation time that turns transient noise analysis. Nevertheless, this technology adds even more advantages to the loop novelty, especially in terms of high switching tunability, and lower power dissipation. Fig.2 shows the fundamental structure diagram of a typical PLL [2, 3].

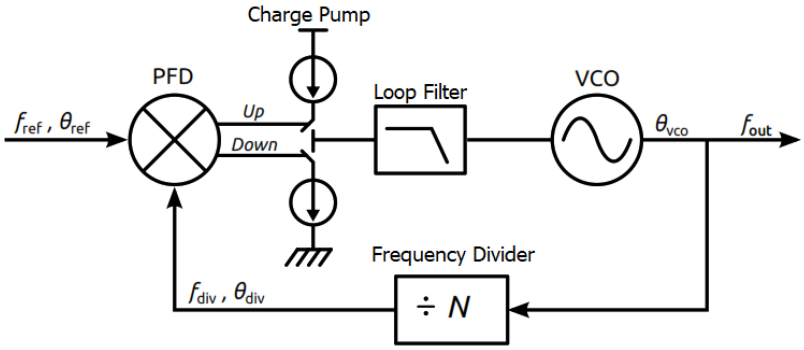

Fig.2. The fundamental structure diagram of a typical PLL

From the PLL rigorous survey of related works and published studies, it is observed that, there have been numerous researchers designed PLLs in their articles and published works. To this end, the number of new works published in the past five years has been pointed out.

M. C. Tripathy et al. reports the realization of an analog fractional□order PLL. The fundamental expressions for lock range, bandwidth, capture range, have been determined analytically and compared with the test result experimentally, they found that, the PLL can provide superior response and phase error at the time of switching compared to its integer□order counterpart [4]. S. Golestan et al. proposed a straightforward viable approach to cut out the errors presented in delay-based PLL, which is called adaptive delay-based PLL (ATD-PLL). The stability evaluation of ATD-PLL and parameter design guidelines are displayed and presented, and the potency of ATD-PLL is confirmed using numerical results [5]. M. Xie et al. presented a new scheme of the PLL circuits, the signal characteristic of phase error is discussed in detail, and the predictive rule is adopted to compensate for the delay induced by moving average filter, thus achieving fast dynamic response [6]. N. V. Kuznetsoy et al. presented a survey of different PLL-based circuits used

in satellite navigation systems, optical, and digital communication, where such difficulties take place in MATLAB and SPICE, is contributed [7]. N. Ikken et al. presents estimated comparisons and analyses of various PLL techniques based on different structures, the results show that the second order generalized integrator-based PLL has a superior performance over other filters-based PLL under both normal and fault operation conditions [8]. J. Yang et al. proposed novel frequency tuning circuits and confirmed in 65 nm CMOS process technology to increase the digital controlled oscillator frequency resolution in order to decrease the reference spurs. They designed a custom varactor and included to the standard cell library, and automatically placed and routed with the standard cells [9]. A. Raj described the effect of execution all digitals PLLs for their application with the analysis of power, area and delay of the synthesizer. The results simulated and synthesized by Xilinx and implemented on FPGA [10]. C. T. Ko et al. proposed a track-and-hold charge pump and automatic control of loop gain, with overcoming of these difficult tasks, it also improves the PLL reference spur performance and jitter [11].

In this study, a novel high-frequency PLL is designed that is applicable for wireless applications. The novel takes advantages from its self-calibration, low phase noise, low sensitivity to environmental changes, and low power dissipation. Using of 22nm CMOS technology is another face of novelty. In CMOS technology, the gate delay is usually taken as a time unit in VCO design which based mostly on the used inverters. The design has very accurate and high-speed frequent turnability, and is limited to a very short dynamic range. The design is applicable for uttermost wireless applications in the band from 2.4 to 5 GHz that is widely used in modern and high-speed wireless devices. The 2.4 GHz band provides coverage at a longer range, although, the 5.0 GHz band provides less coverage but transmits data at faster speeds. Furthermore, the design topology has a great stabilization over this band of frequency.

2. PLL principle, analysis, and &mathematical description

The phase locked loop is an electronic circuit for generating an electrical voltage to synthesize the output signal, its frequency is adaptively adjusted to the input or reference frequency. The input and output frequency relationship is given by,

$$f_{out} = N.f_{in} \tag{1}$$

Where, f_{out} & f_{in} are the output and input frequencies, N is the relative frequency difference (f_{out}/f_{in}) of the PFD signals.
If the VCO and reference signals occur and their corresponding phase reaches in an integer number, the frequency ω_{ref} of reference signal (reference frequency) is usually assumed to be constant,

$$\theta_{ref}(t) = \omega_{ref} t = \frac{t}{T_{ref}} \tag{2}$$

Where, where T_{ref}, ω_{ref} and $\theta_{ref}(t)$ are the period, frequency and phase of reference signal.
PFD is a digital circuit that detects any phase and frequency differences between the input and output signals, and generates control signals to the charge pump (CP) to modulate the amount of charge stored in the low pass filter through the two digital pulses UP and DN. It triggered by the rising edges of reference (f_{ref}) and (f_{VCO}) signals. The output signal of PFD

is *i(t)*, it has only three states as shown in Fig.3, *0*, $+I_p$, and $-I_p$ [12]

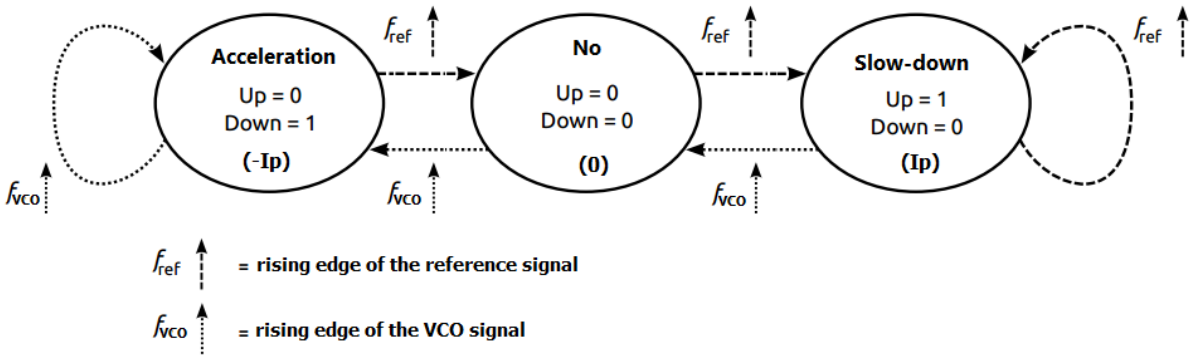

Fig.3. The operational states of the PFD

Both PFD and CP generate current pulses as the phase error (θ_{error}) which represent the phase difference between reference signal (θ_{ref}) and the frequency divider signal (θ_{div}),

$$\theta_{err} = \theta_{ref} - \theta_{div} \tag{3}$$

The issue of the PFD configuration is the phenomenon known as "dead-zone" or " blind-zone", when the phase/frequency difference between input and output signals is close to zero, the width of the UP and DN pulses would approach to a negligible [13], and the CP may not be able to distinguish such definite pulses, hence, no current injecting to the loop filter. As a result, the phase noise (jitter) is incremented. Analogous, given the finite times of leading and ascending edges cause more variations of the PFD in the non-linear region, which is undesirable. The solution is introducing a sufficient delay in the feedback loop to safely reset the UP and DN pulses. However, CMOS logic gates will increase the speed of the PFD circuit and by decreasing reset path delay a higher speed PFD can be designed that has improved as compared to the conventional frequency detectors., and this determines the maximum operating frequency of the PFD. Therefore, adding a delay block is essential to slow down the reset path to be below the switching time of the CP current.

The CP circuit continues UP and DN pulses from PFD to produce a continuous current *i(t)*. Its principle is generally based on controlled charging and discharging of the capacitor in the LF through power sources and controlled switches. In the event when the capacitor is neither discharged nor charged, the voltage remains constant. Thus, the voltage on the capacitor (or filter) ultimately corresponds to the phase/frequency difference of the input signals. Thus, the CP circuit is applied to limit the rate of change of the capacitor's voltage, achieving low phase noise, low spurious output, and the ability to jump from one frequency to the other within a specified amount of time. These characteristics largely depend on the LF, while results are in a slowly rising or falling voltage that depends on the frequency difference from the PFD circuit. The low-pass filter just passes the DC (or low-frequency) component from these pulses. The filtered voltage is then controlled by a voltage-controlled oscillator VCO [14].

The transfer function equations of the PLL are as follows,

$$Open\ Loop\ Gain = G(s).H(S) = \frac{K_d\, F(S)\, K_{VCO}}{s \quad N} \tag{4}$$

$$Closed\ Loop\ Gain = G(s).H(S) = \frac{G(S)}{1 + G(S)\, H(S)} \tag{5}$$

And, the PLL loop response is given by,

$$\frac{q_o}{q_i} = \frac{Ouput\ phase\ in\ radian}{Input\ phase\ in\ radian} = \frac{K_d\ K_{VCO}\ F(S)}{s + K_d\ K_{VCO}\ F(S)} \tag{6}$$

Where, K_d is the PFD gain (V/radian), K_{VCO} is the VCO gain (radian/V.sec), $F(S)$ is the loop filter transfer function.

In practice, 2nd order filters are most used because of its simplicity, inherent stability, and offer better noise cancellation, and is used in most of the computer and communication systems. The LF response for a second order PLL is given by,

$$\frac{q_o}{q_i} = \frac{\frac{K_d\ K_{VCO}}{RC}}{s^2 + \frac{s}{RC} + \frac{K_d\ K_{VCO}}{RC}} \tag{7}$$

Where, RC is the time constant and determine the frequency range of VCO, another optional resistor can be added in parallel with RC to ensures that, the VCO has a certain frequency offset when necessary. The VCO design has high input impedance facilitates when selecting the low-pass filter; this offers the designer a wide selection of RC values. The standard second order transfer function is [15],

$$T(S) = \frac{S^2}{S^2 + 2\,\zeta\,\omega_n\,s + \omega_n{}^2} \tag{8}$$

Therefore, the damping ration (ξ), and natural frequency (ω_n) is given by,

$$\zeta = \frac{1}{\sqrt{K_d\ K_{VCO}\ RC}},\ \omega_n = \sqrt{K_d\ K_{VCO}/RC} \tag{9}$$

For a second-order system, ω_n and ξ are formulated to redefine the transfer function,

$$\zeta = \frac{\omega_n}{2} RC,\ \omega_n = \frac{K_d\ K_{VCO}}{N\ C} \tag{10}$$

The relationship between natural frequency (ω_n) and loop BW in terms of DC is written as,

$$\omega_c = 2\,\zeta\,\omega_n \tag{11}$$

Assume frequency division ratio *is "1"* to simplify the calculations, the closed response can be given as,

$$Fout(S) = \frac{1}{s} + \frac{-s}{s^2 + 2\,\zeta\,\omega_n\,s + \omega_n{}^2} \tag{12}$$

First, the damping factor (mainly 0707) and the filter bandwidth are chosen, then the natural frequency can be found. Therefore, the value of R and C can be found to complete the transfer function of the designed loop,

$$C = \frac{I.K_{VCO}}{2\pi N\,\omega_n{}^2},\ R = 2\zeta\sqrt{\frac{2\pi N}{I\,K_{VCO}\,C}} = \zeta\frac{4\pi N\,\omega_n}{I\,K_{VCO}} \tag{13}$$

Thus, the PLL system may be characterized by its transfer functions to expresses the output signal of the linear system. On the other hand, applying a lower nanotechnology process minimize total power consumption of the PLL.

3. The PLL Novelty metrics

The PLL novelty characterized based on; low phase noise, low jitter, low sensitivity to environmental changes, low power dissipation, and a wide PLL turnability over the chosen band of frequency.

Noise is defined by random fluctuations in the period of the output signal. Phase noise which is measured in (dBc/Hz) plays a vital role in the PLL systems and significantly affecting its performance. Mainly, the phase of the PFD signals is fluctuating when compared to the ideal signal. As a result, the phase noise is produced, which is very intense. Phase noise as shown in Fig.4 in a CMOS PLLs is modelled from its building blocks. The reliability issues pose challenges to designers to go through deep submicron CMOS technologies to develop a better signal to noise ratio which is required for uttermost wireless applications and high-speed wireless devices. In addition, phase noise as well as jitter both performs the stability of a signal, while Jitter is the random phase variation of a timing signal from its ideal positions due to environmental and circuit noise, it has the same physical relation as the phase noise, its measured in units of root-mean-square (RMS) seconds. Jitter can be classified as cumulative, periodic and cycle to cycle jitter [16].

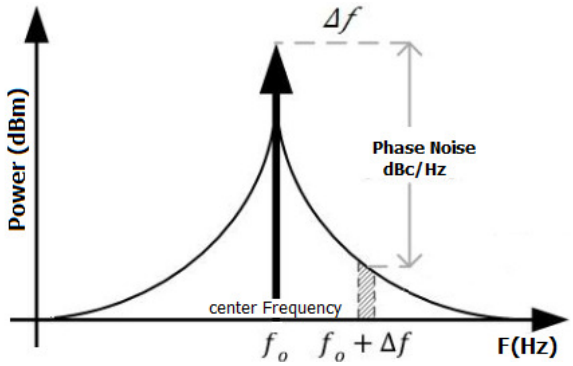

Fig.4. The phase noise

First, sources of jitter must be constructed, Jitter is mainly caused by device mismatches and non-ideal input clock effects such as jitter and duty cycle errors., another source is thermal, substrate, and power supply noise. Therefore, minimize timing errors leads to obtain a low jitter PLL [17].

The phase-noise or jitter of a PLL output signal is caused by a combination of all the random noise sources in the system; noise of the reference signal, PFD, CP noise, LF, VCO, and divider noise. If the input/ reference signal is stable, the VCO's output signal will be stable significantly, and thus the PFD signals been stable and precise frequency is generated.

Another PLL design challenges in the Nano process CMOS technology is reference spurs due to a leakage current of a loop filter capacitor. Reference spurs cheapen timing accuracy as well as spectral purity of the PLL output, and PFD provides the wider UP pulse. Spurs as the phase noise also lead to unwanted change in the output frequency and cause deterministic variations with specific amplitudes and frequencies as shown in Fig.5 [18].

Typically, there are dominant jitter and noise contribution in GHz ranges in wireless devices. The phase noise and variation in phases which is called as tracking jitter. Practically, in the design choices, the phase error should be equal to zero and the jitter should take as small values as possible. It is often necessary for the PLL circuit designers to specify allowed noise at the PLL input that makes the PLL output to meet its specification. Many researches recommended that, using a low bandwidth PLL is useful in filtering the noise. However, using low bandwidth PLL is not always advantageous to use because the relative contribution of VCO noise to a PLL's output jitter increases as the loop bandwidth decreases. Therefore, a trade-off decision is appearing. The PLL bandwidth needs to be set to minimize noise and reference jitter, and it is mainly depending on the application to make the decision and needs verification independently on the simulation of a practical design [19].

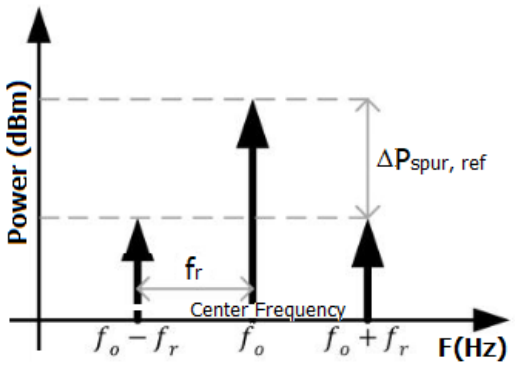

Fig.5. The reference spurs

It is also important to address the tunability of the PLL circuit. The PFD utilizes the reference or input signal to tune the VCO and, in the lock state, it must be equal to the desired output frequency, when the frequency divider changes the value N, the VCO can be tuned across the used frequency band. Hence, the minimum frequency resolution, or channel spacing sections are very important parameters. Channel spacing is given by,

$$ChannelSpacing = \frac{f_{VCO}}{N} \tag{14}$$

In the unlock state of the PLL, PFD will create an error voltage signal on the difference of the frequency or phase values between the two input signals and leads to tuning the VCO output frequency until the system is reached the lock state. This is mainly obtained by adding internal circuitry that enables the value of N to change dynamically during the locked state. If the value of the divider is "switched" between N and N+1 in the correct proportion, this allows the PFD to run at a frequency that is higher than the PLL channel spacing. In the presented design, the frequency of the inverter ring oscillator easily could be adjusted by controlling the supply of the inverters. The voltage-to-frequency conversion over a large range of frequency will be smoothly linear, and the voltage gain of the

oscillator will be relatively constant, and VCO should be directly proportional to the applied control voltage, its mathematical equation is [20],

$$\omega_{out} = w_o + K_{VCO} * V_{ctrl} \quad (15)$$

ω_o is the free running frequency and K_{VCO} is the slope of the VCO frequency response and is also the gain of the VCO system. The VCO will be linear as possible, so that the output frequency increases or decreases linearly with respect to V_{ctrl}. The range of frequency over which the VCO works is called a tuning range. Using two controllable CP circuits will adjust the loop gain and increase the VCO tuning range when necessary. The V_{ctrl} of VCO range is controlled by the supply voltage levels which is necessary to keep the charge pump in saturation. Therefore, the V_{ctrl} is limited to the minimum value of a saturation voltage from the supply rails.
Fig.6 shows linear characteristics of a VCO.

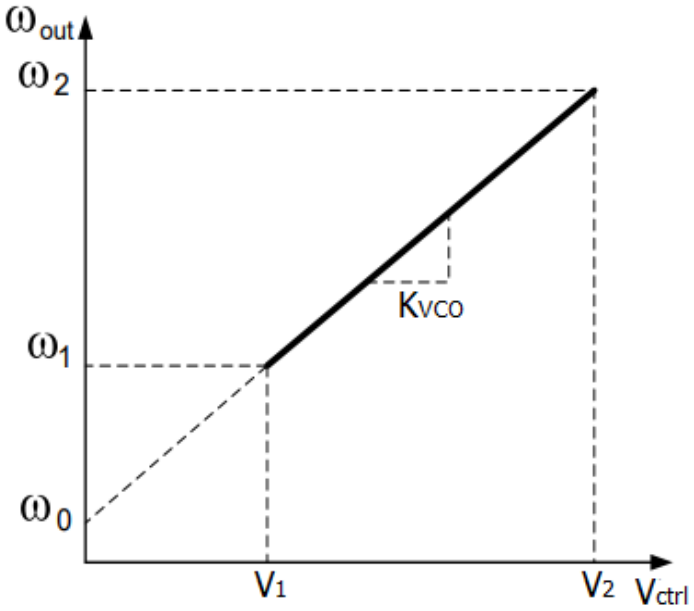

Fig.6. The VCO linear characteristics

In spite of this, the PLL self-calibrating objectives tends to minimize the effects of supply voltage, and temperature variations. Researches designed the self-calibrating circuit to operate with a power supply range and to operate across the temperature range. On the other hand, meticulous discipline, design, and practical experience can take advantage as a substitute for extra and complicated circuits to address any transients and new environmental conditions.

PLLs primarily suffer from trade-offs between dynamic output range, switching speed, power dissipation and noise. Thus, power dissipation is another important aspect of PLL design. Lower power dissipation increases the overall PLL speed and improves the noise effect. The designed PLL circuit deals very seriously with the power dissipation problem. Furthermore, it solves the dead-zone and missing edge problems altogether. Commonly, power dissipation at the transient time of switching transistors and during active time or simultaneously is very crucial [21].

The measurement for a low power PLL for wireless applications is designed in 22 in nm CMOS technology. For low power, low leakage transistors will be used and dynamic supply voltage scaling (DVS) is applied, which is consistent in allowing compact efficient thermal control and low power consumption of PLLs. The DVS is applied perfectly for the integrated combination of PLL blocks to modulate the PLL circuit to its optimal power dissipation. Monitoring the transistor's temperatures is the efficient algorithm to scale the supply voltage accordingly. Moreover, the PLL functionality is also verified for the lower supply voltages from 1.2 V down to 1.0 V.

The power dissipated in a PLL circuit is composed of dynamic switching power, and static leakage power. The dynamic part of the dissipated power is dominant and has larger contributor. Power reduction strategies can be used to minimize both types of power. The VCO is the most conspicuous functional block in the PLL, it dissipates the main power in the PLL system. Obviously, this block is a particular focus on the minimization of power dissipation. VCO for a GHz frequency range and critical power dissipation of a Nano process CMOS technology with good phase noise performance can be achieved through the DVS technique. The dynamic power depends on quadratic VDD in a quadratic relation, since it is proportional to ($C_{eff}.VDD^2.f$). The reduction of VDD brings a strong reduction in dynamic power, while maintaining the of possibility increasing the maximum frequency at the VCO output [22],

$$T_p = \alpha \frac{C_{eff}\, VDD}{(VDD - V_{th})^2} \tag{16}$$

$$P_{dynamic} = \alpha\, f\, C_{eff}\, VDD^2 \tag{17}$$

Where T_p is the VCO inverter time delay, α is the switching activity, VDD is the supply voltage, C_{eff} is the inverter effective load capacitance, V_{th} is the transistor threshold voltage, and f is the frequency.

The VDD scaling is the technique that has the greatest impact on reducing total power. Fig.7 shows the total power of a 0.13µm CMOS ring oscillator, over a scale of VDD and constant clock frequency.

Dynamic power dissipation can be minimized by reducing switching activity and clock frequency, which affects the PLL system performance; and also, by reducing effective load capacitance of the VCO inverter chain and supply voltage. Supply voltage scaling is more effective and has a quadratic effect on dynamic power. Dynamic power can also be reduced by cell selection, faster slew cells consume less dynamic power. In another view, there is an optimum supply voltage VDD and V_{th}. Below this optimum, the reduction in dynamic power dissipation becomes inefficient as the static power dissipation becomes considerable. This optimum point also depends on the activity factor of the circuit [22, 23].

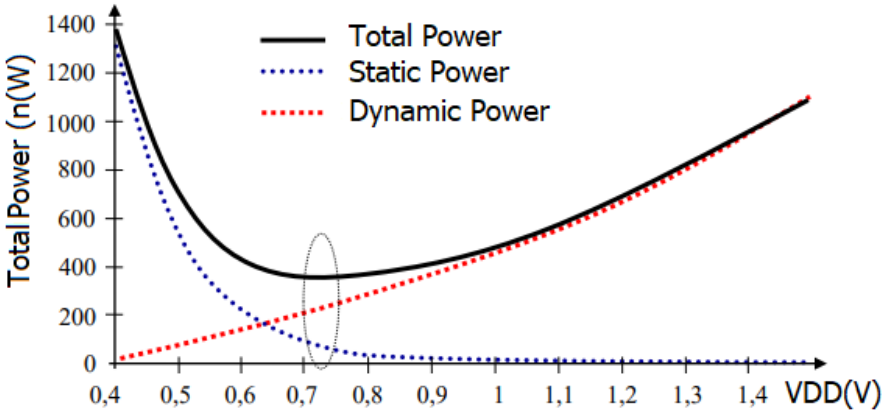

Fig.7. Total power of CMOS ring oscillator (0.13 µm) over a scale of VDD and constant clock frequency.

Without scaling the supply voltage, power dissipation can be minimized through frequency scaling, but the total energy consumption per operation remains the same. Dynamic voltage scaling contributes directly to energy consumption reduction, where the dynamic energy consumption of a gate is a direct function of the square of supply voltage, DVS can be applied at different interval of time according to the temperature circumstances which helps to reduce the power dissipation. In addition, it provides dynamic thermal management for the PLL system for different levels of the PLL performance granularity [24].

4. The Novel PLL Design

PLL is a complex system and it is required observation of the design levels and ensure correct parameters. For low phase noise, low jitter, low sensitivity to environmental changes, and low power dissipation, the design of a second order CMOS PLL is presented in this study for a wide PLL turnability over the chosen frequency band 2.4-5.0 GHz and supply voltage 1.0-1.2V using 22nm technology. These specifications are applicable for uttermost wireless applications and widely used in modern and high-speed wireless devices.

PFD compares the phase and frequency of the reference and VCO or divider signals and determines the output, it detects the timing difference of the input signal only at the rising edges. The PFD circuit ideal and actual characteristics are shown in Fig.8, [25].

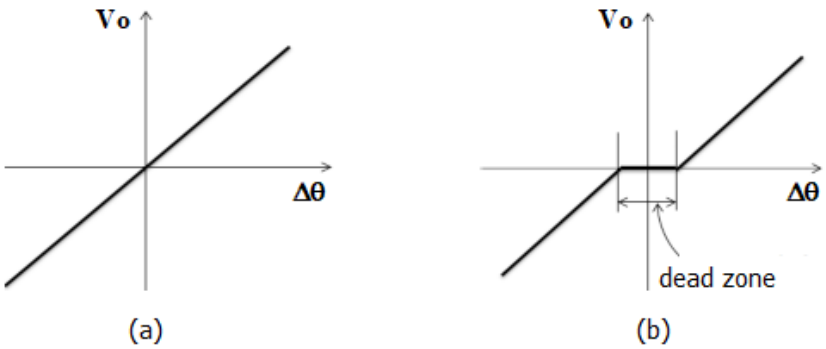

Fig.8. PFD Characteristics, (a) Ideal, (b) Actual

As previously explained, a dead-zone which is shown above has appeared when the width of UP and DN pulses approaching to minimum, the charge pump may not be able to detect such narrow pulses, resulting to no current injecting to the loop filter. As a result, the phase noise (jitter) will increase. For this reason, a delay block was added to the path of the reset signal to slow down the reset path to be below switching time of the CP current. Hence, the pulse width of the UP-DN signal is sufficiently wide and the dead zone disappeared. Phase noise as the total noise contributed to the PFD from the input signal, these include transistors, reset time, and dead zone. The presented PFD circuit is reliable and well improved the mentioned complications, and provides minimum phase noise and jitter.
The PFD circuit diagram is shown in Fig.9.

The role of CP is converting the PFD digital outputs to analog signals as charge flows. The width of UP/DN pulses with a width equal to the phase/frequency difference between the PFD inputs. Thus, the CP is used to sink and source current into the LF. The charge pump current is given by,

$$I_{cp} = K_d.\Delta\varphi, \quad K_d = \frac{Ipump}{2\pi}(\text{amps/ radians}) \qquad (18)$$

Thus, it is important to design a CP circuit that has equivalent pull-up and pull-down currents as per PFD switching times to bypass any static-phase offset that causes ripples in the control voltage, thereby creating a "jittery" on VCO output clock. Bootstrapped CP design is used, which allows differential current steering, and it can operate with low-swing UP/DN signals. Thus, it is very prominent for PLLs that use high-frequency signals. The loop filter converts the current from the CP to a voltage. The high frequencies lead to generating an oscillation of the pumped current from CP circuit. Therefore, the loop requires a LF to convert this oscillation to a stable voltage quickly. The circuit diagram of the CP-LF is shown in Fig.10.

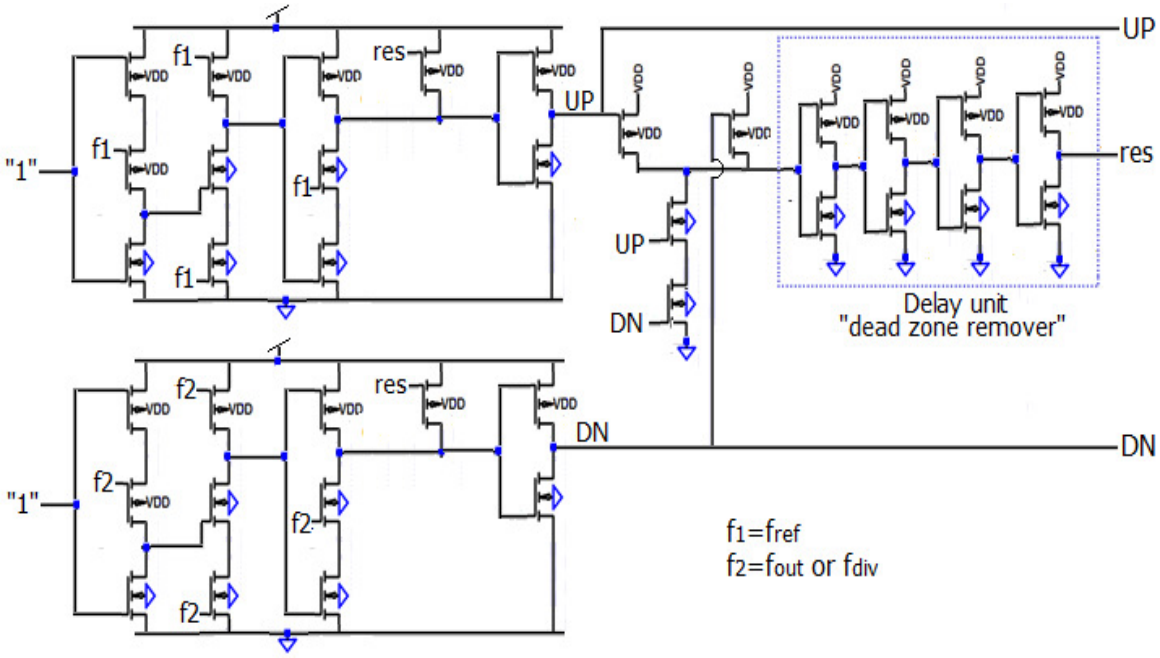

Fig.9. The PFD circuit diagram

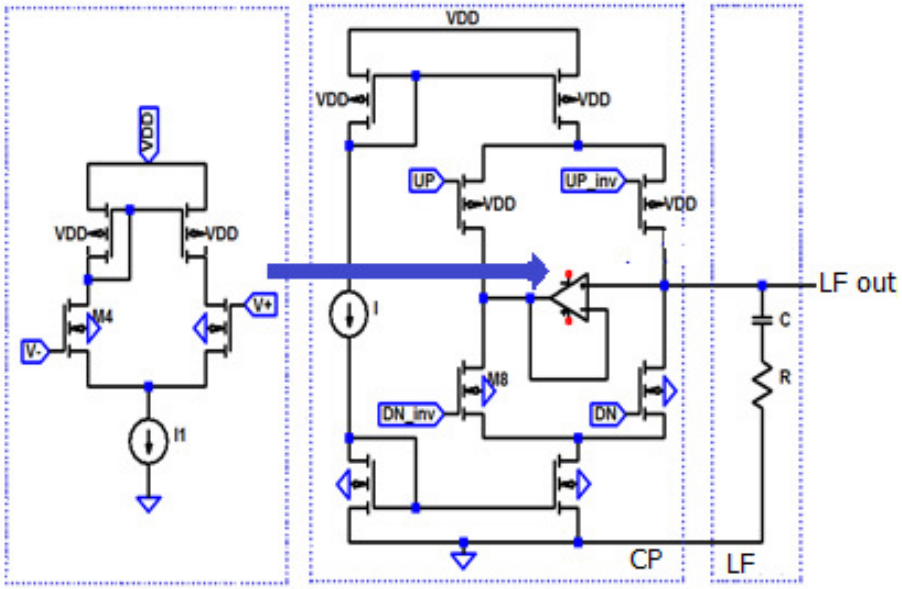

Fig.10. The CP-LF circuit diagram

The oscillation frequency of the current-starved VCO for N_s (an odd number) of stages is ($f_{osc}=1/(N_s .C_s.V_{ctrl})$ and maximum and minimum frequencies are determined by (V_{max}=VDD), and ($V_{min}=V_{th}$).

Total 7 stages are required to generate 2.4-5.0 GHz, the configuration of the simulation model of the CS-VCO is shown in Fig.11. The control voltage (V_{ctrl}) drives this current source, and the current will determine the charge up and discharge time of the inverter. This topology is called current-starved inverter; the current sources limit the current available to the inverter. In other words, the inverter is starved for current. The CS-VCO is preferred because it is superior in term of power dissipation, smaller chip area, power consumption, good tuning range, and oscillation frequency can achieve reasonably fast. The design is suitable for high-frequency PLLs [26].

In high-frequency wireless applications and devices, frequency divider (FD) is a critical part of the PLL circuit. Commonly, the VCO frequency is in order of several GHz, from here the frequency needs to be divided. The simplest way to implement a clock frequency division is to design a digital counter, with a digital logic resetting the counter after a number of input cycles equal to the division ratio have been counted. If the value of the divider is "switched" between N and N+1 in the correct proportion, this will allow the PFD circuit to run at a clock frequency that is higher than the PLL channel capacity.

The VCO generates a required clock frequency to support the PLL output. The frequency divided is used to match with reference frequency in the locked state. The divider acting on same factor with VCO for a possible VCO frequency division. Simply D flip flop (D-FF) used as a frequency divider. Each D-FF produces a divide by-2. Therefore, design divider in any order will depend on the chain of the D-FF. The structure of the frequency divider is made of four D-FF chains each as a divider by-2. In order to select the division ratio, a programmable multiplexer has been added using two control signals S_1 and S_2, at any instant, a possible division ratio is selected, 2, 4, 8, or 16. Fig.12 shows the structure of D-FF as a frequency divider by-2. The structure of frequency divider is shown in Fig.13 [25].

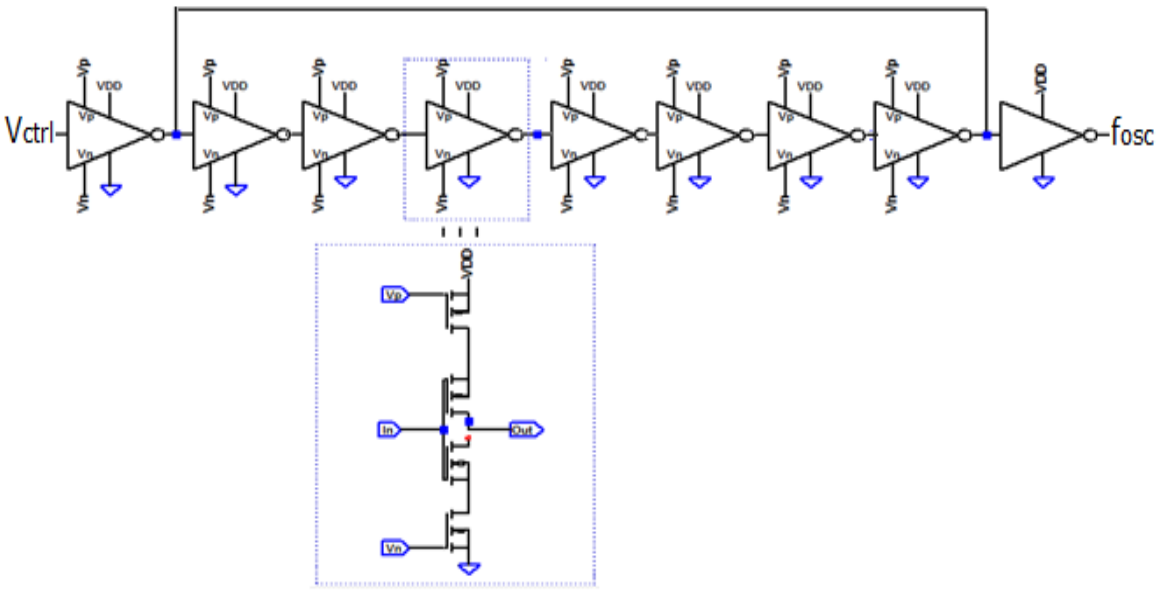

Fig.11. The 7-stages CS-VCO

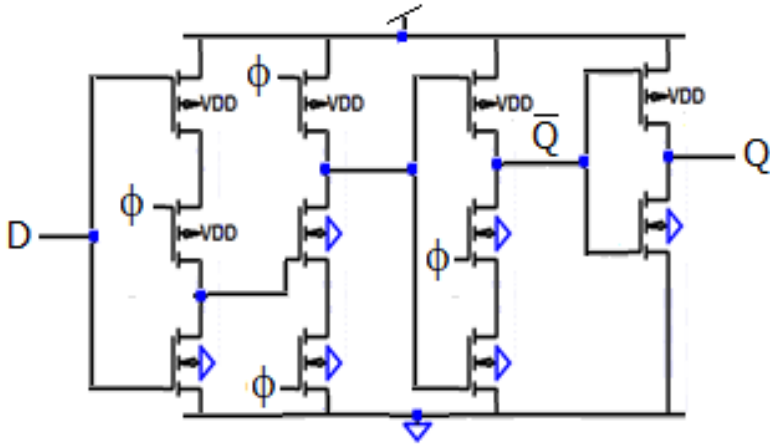

Fig.12. The structure of the D-FF as a frequency divide by-2

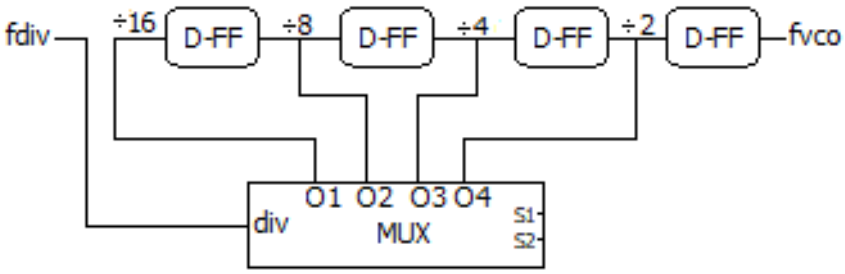

Fig.13. The structure of frequency divider

The recent advances in wireless applications and the rapid increase in operating frequencies, and the possibility of high-frequency PLLs what made the design followed in this study and schematic topologies that interpreted here can be applied to a wide variety of high performance and high speed PLL applications, it is worthwhile paying special consideration to wireless devices. The design is preferred for its simplicity, low phase noise, low jitter, low sensitivity to environmental changes, and low power dissipation. The attention on the addressed issues in this study is significant and has the possibility of

expanding to the design of future high speed and low power PLLs into low-noise multi-GHz applications in all modern communication devices.

5. Simulation & results

This section presents the results carried out on the presented design circuits to estimate the novelty of the designed PLL, a SPICE simulation environment for 22 nm CMOS technology is used. The design consists of a transistor-level phase-frequency detector (PFD), charge pump (CP), loop filter (LF), a voltage-controlled oscillator (VCO), and frequency divider (FD), rather than the design verification for wireless frequency band of 2.4-5.0 GHz band. Moreover, the PLL design functionality is also verified for a scale of supply voltages from 1.0 V up to 1.2 V.

The figures shows samples of the resultant plots. Fig.14 (a) shows the PFD output pulses when f_{ref} is higher than f_{out}, UP pulses are appeared, Fig.14 (b) shows the PFD output pulses when f_{out} is higher than f_{ref}, DN pulses are appeared, Fig.14 (c) shows the PFD output pulses at lock state, which generated a constant control voltage (V_{ctrl}) to the VCO equal to 1.089V that produced a centre frequency of 3.70 GHz. Fig.15 shows the VCO output frequency at f_{centre}=3.70GHz. Fig.16 shows the CP output at f_{centre}=3.70GHz. Fig.17 shows the LF output at f_{centre}=3.70GHz.

The tables showing the simulation results. The Frequency band & LF Parameter is shown in Table 1. The phase noise analysis in shown Table 2. The frequency and noise jitter analysis in shown Table 3. The properties of UP and DN pulses is shown in Table 4. The PLL performance analysis is shown in Table 5. The PLL power consumption is shown in Table 6.

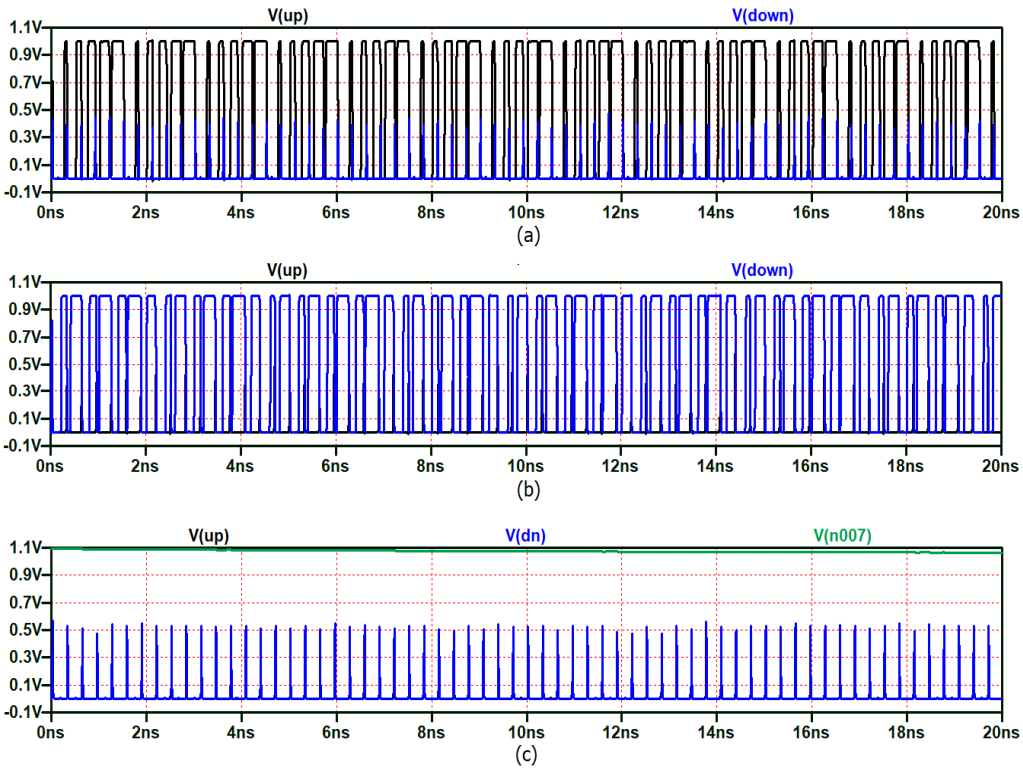

Fig.14. The PFD output pulses, (a) f_{ref} is higher, (b) f_{out} is higher, (c) lock state, V_{ctrl}=1.089V

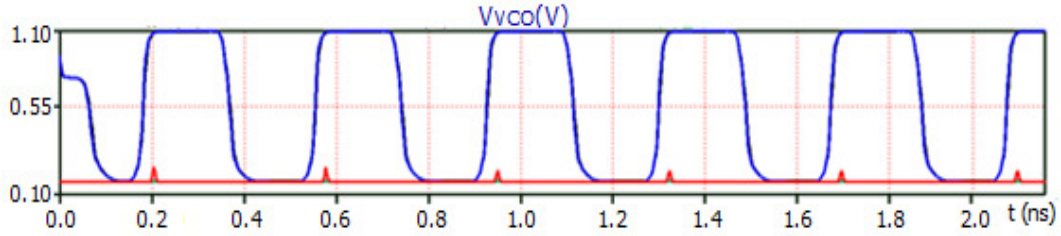

Fig.15. The VCO output at lock state, f_{centre}=3.70GHz

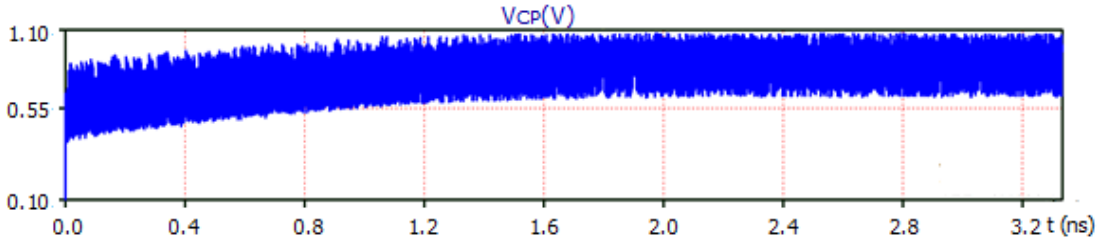

Fig.16. The CP output, f_{centre}=3.70GHz

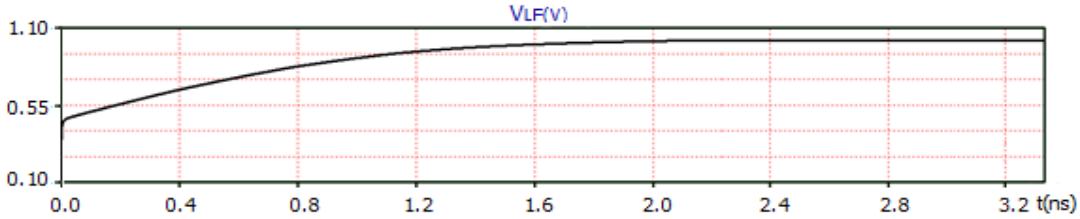

Fig.17. The LF output, f_{centre}=3.70GHz

Table 1: Frequency Band & LF Parameter

Process (nm)	22
Frequency band (GHz)	2.4-5.0
Centre frequency (GHz)	3.70
Supply Voltage (V)	1.0-1.2
VCO divider	2
Tracking Range (MHz)	100
Capture Range (MHz)	50
R (KΩ)	55
C (nF)	67.28

Table 2: The phase noise

F (Hz)	Phase Noise (dBc/Hz)		
	Total Filter	VCO	PLL
1.000M	-118.7	-121.5	-137.6
10.00M	-137.3	-140.7	-166.0
100.0M	-161.1	-164.6	-194.5
1.000G	-188.6	-191.9	-220.1
2.000G	-201.4	-206.7	-233.8
3.7.00G	-211.9	-215.1	-245.4
5.000G	-216.2	-219.6	-252.9

Table 3: Frequency & Noise Jitter

Noise & Jitter	350 dBc
Phase Jitter (1kHz-100MHz)	12.5 ps rms
Frequency Locking	381 us – 575 us
Supply Voltage (V)	1.0-1.2
Lock Detect Threshold	1.0 V

Table 4: UP & DN Pulses

DC Voltage (V)	1.1
Delay (ps)	15
Rise Time (ps)	0.15
Fall Time (ps)	0.15
Lock Detect Threshold (V)	1.0

Table 5: The PLL Performance

Random Jitter from VCO (worst case, RMS, ps)	<1
Deterministic jitter (peak-peak, ps)	1.84
Voltage swing/VDD	75.21%
Current Mismatch	<1%

Table 6: The PLL Power Consumption

Power Supply (V)	Power Consumption (µW)
1.0	135.673
1.1	148.546
1.2	190.252

The above resultant tables indicating that, the PLL design is a fully integrated and has excellent characteristics. The power consumption of approximately 135.67-190.25 µW. The operating frequency band of the PLL is 2.4-5.0 GHz designated for the supply scaling voltages from 1.0V to1.2V. It has an excellent voltage swing per *V*DD (75.21%), while its power consumption is reasonable in the centre frequency of 3.70 GHz.
The PLL design is efficient and allows the rapid determination of switching speed to evaluate the frequency division ratio for a low power specification while monitoring the transient performance in the time domain instantaneously.

6. Conclusion

The aim of this work was a transistor level design of a novel PLL as a feedback control system, using 22 nm CMOS process technology for a wide band of 2.4-5.0 GHz, applicable in wireless applications. The key to design novelty is characterized by; lower phase noise, low jitter, low sensitivity to environmental changes, low power dissipation, and a wide PLL turnability over the chosen band of frequency. The design functionality was verified by SPICE simulation through transient and noise analyses.

The scale of the supply voltage was 1.0-1.2 V, the tracking and capture ranges was 100MHz and 50MHz respectively. The frequency locking time was 381-575us, and the current mismatch was less than "1". It is also important to point out that, the entire circuit power consumption is about 135.67-190.25 µW for the mentioned scale of the supply voltages. Finally, the design is able to lock in a high-speed time and with excellent tuneable range, and it has a good potential for the devices operating in the wireless band.

In addition, the design and circuit structures are accurate, comprehensive, and meets the average specifications and requirements of a proper PLL capable of using in lots of devices operating in the wireless band. Besides, results confirmed that, the design is able to successfully improve performance specifications with the scaled supply voltage technique. The followed procedure allows one to significantly reducing time required for numerical measurements to determine important features, design and simulation model. Therefore, the presented design can be considered as a proper design constraint for current and future devices operating in the wireless band.

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